THAT WHICH IS CLAIMED IS:

1. A method of fabricating an integrated circuit device comprising:

forming a conductive layer on a microelectronic substrate;

forming an insulating layer on the conductive layer, the insulating layer including an overhanging portion that extends beyond the conductive layer; and

forming a sidewall insulating region disposed laterally adjacent a sidewall of the conductive layer and extending between the overhanging portion of the insulating layer and the microelectronic substrate.

2. A method according to Claim 1, further comprising:

forming an insulating region between the overhanging portion of the insulating layer and the microelectronic substrate; and

forming a sidewall spacer conforming to a sidewall of the insulating layer, the sidewall insulating region and an adjoining surface of the insulating region.

3. A method according to Claim 1, wherein forming the conductive layer comprises forming the conductive layer by adjusting the etchant so that the insulating layer includes the overhanging portion that extends beyond the conductive layer.

4. A method according to Claim 1, wherein forming the conductive layer comprises forming a conductive layer having first and second metallic layers.

5. A method of fabricating a self-aligned contact structure for a microelectronic device, the structure comprising:

forming a conductive layer on a microelectronic substrate;

forming an insulating layer on the conductive layer, the insulating layer including an overhanging portion that extends beyond the conductive layer;

forming a sidewall insulating region disposed laterally adjacent a sidewall of the conductive layer and extending between the overhanging portion of the insulating layer and the microelectronic substrate; and

forming a conductive region disposed laterally adjacent the sidewall insulating region such that the sidewall insulating region separates the sidewall of the conductive layer and the conductive region.

6. A method according to Claim 5, further comprising:

forming an insulating region between the overhanging portion of the insulating layer and the microelectronic substrate; and

forming an insulating sidewall spacer conforming to a sidewall of the insulating layer, the sidewall insulating region and an adjoining surface of the insulating region, wherein the conductive region is laterally adjacent the insulating sidewall spacer.

7. A method according to Claim 5, wherein forming the conductive layer comprises forming the conductive layer by adjusting the etchant so that the insulating layer includes the overhanging portion that extends beyond the conductive layer.

8. A method according to Claim 5, wherein forming the conductive layer comprises forming a conductive layer having first and second metallic layers.

9. A method of fabricating an integrated circuit memory device, comprising:

forming a first bit line comprising:

forming a first conductive layer on a microelectronic substrate;

forming a first insulating layer on the first conductive layer, the first insulating layer including a first overhanging portion that extends beyond the first conductive layer; and

forming a first sidewall insulating region disposed laterally adjacent a first sidewall of the first conductive layer and extending between the first overhanging portion of the first insulating layer and the microelectronic substrate; and

forming a second bit line comprising:

forming a second conductive layer on a microelectronic substrate;

forming a second insulating layer on the second conductive layer, the second insulating layer including a second overhanging portion that extends beyond the second conductive layer; and

forming a second sidewall insulating region disposed laterally adjacent a second sidewall of the second conductive layer and extending between the second overhanging portion of the second insulating layer and the microelectronic substrate.

10. A method according to Claim 9:

wherein the forming the first bit line further comprises:

forming a first insulating region disposed between the first overhanging portion of the first insulating layer and the microelectronic substrate; and

forming a first sidewall spacer conforming to a sidewall of the first insulating layer, the first sidewall insulating region and an adjoining surface of the first insulating region; and

wherein forming the second bit line further comprises:

forming a second insulating region disposed between the second overhanging portion of the second insulating layer and the microelectronic substrate; and

forming a second sidewall spacer conforming to a sidewall of the second insulating layer, the second sidewall insulating region and an adjoining surface of the second insulating region.

11. A method according to Claim 9:

wherein forming the first conductive layer comprises forming the first conductive layer by adjusting the etchant so that the first insulating layer includes the overhanging portion that extends beyond the first conductive layer; and

wherein forming the second conductive layer comprises forming the second conductive layer by adjusting the etchant so that the second insulating layer includes the overhanging portion that extends beyond the second conductive layer.

12. A method according to Claim 9:

wherein forming the first conductive layer comprises forming the conductive layer having first and second metallic layers; and

wherein forming the second conductive layer comprises forming the second conductive layer having third and fourth metallic layers.